Patent

Customer No.: 31561
Docket No. 10544-US-PA
Application No.: 10/709,179

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of	
Applicant	: Chang et al.
Application No.	: 10/709,179
Filed	: April 19, 2004
For	: STACK-TYPE MULTI-CHIP PACKAGE AND METHOD OF FABRICATING BUMPS ON THE BACKSIDE OF A CHIP
Art Unit	: 2814
Examiner	: HA, NATHAN W.

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Assistant Commissioner for Patent
Alexandria, VA 22314

In response to the Examiner's Answer on July 10, 2006, please find the *Reply Brief* in 17 pages.

The Commissioner is authorized to charge any fees required in connection with the filing of this paper to account No.: 50-2620 (Order No.: 10544-US-PA).

Thank you for your assistance in the subject matter. If you have any questions, please feel free to contact me.

Respectfully Submitted,
JIANQ CHYUN Intellectual Property Office

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

EX PARTE Chang et al.

Application for Patent

Filed: April 19, 2004

Serial No. 10/709,179

FOR:

STACK-TYPE MULTI-CHIP PACKAGE AND METHOD OF FABRICATING BUMPS ON THE BACKSIDE OF A CHIP

(as amended)

REPLY BRIEF

JIANQ CHYUN Intellectual Property
Attorneys for Applicants

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I. Real party in interest

The real party in interest is Advanced Semiconductor Engineering, Inc., the assignee of record.

II. Related appeals and interferences

There are no related appeals and/or interferences.

III. Status of the claims

A total of 20 claims were presented during prosecution of this application. Claims 1-14 have been cancelled. The Applicant appeals the rejected claims 15-20.

IV. Status of amendments

There has been an amendment to the independent claim 15 filed subsequent to the final rejection. However, the amendment was not entered.

V. Summary of claimed subject matter

The claimed subject matter of the present invention involved in the appeal is directed to a method of fabricating bumps on a backside of a chip. The method comprises providing the chip 320 with an active surface 321 having at least a bonding pad thereon 322 as shown in Figure 4A and as discussed in [0029], [0034]. The chip 320 is also formed with at least a bump pad 380 on the backside 327 of the chip 320 (please refer to Figures 4E-4F and [0029], [0036]). A bump 390 is further formed on the bump pad 380 on the backside of the chip 320 as shown in Figure 5A-5B and [0029], [0037]. Additionally, claims 16 and 17 further teaches the step of forming the bump pad on the backside of the chip. Claim 16 teaches that the bump pad is formed by forming a metallic layer on the backside of the chip and patterning the metallic layer to form the bump pad as shown in Figures 4C-4E, while claim 17 teaches

the bump pad is formed by putting a mask on the backside of the chip, wherein the mask has at least an opening to expose the backside of the chip as shown in Figure 6A and forming a metallic layer over the mask and the exposed backside of the chip as shown in Figure 6B, followed by removing the mask so that the remaining metallic layer on the backside of the chip becomes the bump pad as illustrated in Figure 6C.

VI. Grounds of rejection to be reviewed on appeal

Were claims 15-16, 18 properly rejected under 35 U.S.C. 102(e) as being anticipated by Ono et al. (US 2003/0107129)?

Were claims 17 and 19 properly rejected under 35 U.S.C. 103(a) as being unpatentable over Ono as applied to claims 15-16 above, and further in view of Akram (US 6,861,763)?

Was claim 20 properly rejected under 35 U.S.C. 103(a) as being unpatentable over Ono as applied to claims 15-16 above, and further in view of Koh (US 2004/0135266)?

VII. Arguments

A. The related law

In order to properly anticipate Applicants' claimed invention under 35 U.S.C.§ 102, each and every element of the claim in issue must be found "either expressly or inherently described, in a single prior art reference." "The identical invention must be shown as complete detail as is contained in the ...claim Richardson v. Suzuki Motor Co., 868 F. 2d 1226, 1236, 9USPQ2d 1913, 1920 (Fed. Cir. 1989)." See M.P.E.P § 2131, 8th ed., 2001.

The standard for lack of novelty is one of strict identity. To anticipate a claim for a patent, a single prior source must contain all its essential elements. *Hybritech Inc. v. Monoclonal Antibodies, Inc.*, 802 F.2d 1367, 231 U.S.P.Q. 81, 90 (Fed. Cir. 1986).

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. V. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

For a prior art reference to anticipate in terms of 35 U.S.C. § 102, every element of the claimed invention must be identically shown in a single reference. ..... These elements must be arranged as in the claim under review. *In re Bond*, 910, F. 2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990).

The inquiry as to anticipation is symmetrical with the inquiry as to infringement of a patent. A classic test of anticipation provides : That which will infringe, if later, will anticipate, if earlier. *Knapp v. Morss*, 150 U.S. 221, 37 L. Ed. 1059, 14 S. Ct. 81 (1893); *Lindermann Maschinenfabrik GMBH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 1459, 221 U.S.P.Q. 481 (Fed. Cir. 1984). Therefore, **by analogy, the all elements rule used for a determination of infringement finds its applicability in a determination of anticipation**. Discussion of the all elements rule can be found in *Becton Dickinson and Co. v. C.R. Bard Inc.*, 17 U.S.P.Q. 2d 1962, 1967 (Fed. Cir 1989) and *Hi-Life Products Inc. v. American National Water-Mattress Corp.*, 6 U.S.P.Q.2d 1132, 1133 (Fed. Cir. 1988).

To establish a prima facie case of obviousness under 35 U.S.C. § 103(a), each of three requirements must be met. First, the reference or references, taken alone or combined, must teach or suggest each and every element recited in the claims. Second, there must be suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to combine the references in a manner resulting in the claimed invention. Third, a reasonable expectation of success must exist. Moreover, each of the three requirements must "be found in the prior art, and not be based on applicant's disclosure." MPEP § 2143, 8th ed., February 2003.

A claimed invention is unpatentable if the differences between it and the prior art "are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art." 35 U.S.C § 103(a); see *Graham v. John Deere Co.*, 383 U.S. 1, 14, 86 S. Ct. 684, 15 L.Ed.2d 545, 148 USPQ 459, 465 (1966).

"The inquiry is not whether each element existed in the prior art, but whether the prior art made obvious the invention as a whole for which patentability is claimed." Hartness

International, Inc. Vs. Simplimatic Engineering Co., 819 F2d 1100, 1108, 2 USPQ 2D 1826 (Fed. Cir. 1987).

To establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974).

There must be some motivation to combine the references; this motivation must come from "the nature of the problem to be solved, the teachings of the prior art, [or] the knowledge of persons of ordinary skill in the art." *In re Rouffet*, 149 F.3d 1350, 1357, 47 USPQ2d 1453, 1457-58 (Fed. Cir. 1998).

"Combining prior art references without evidence of such a suggestion, teaching, or motivation simply takes the inventor's disclosure as a blue print for piecing together the prior art to defeat patentability—the essence of hindsight". *In re Dembiczak*, 175 F.3d at 999.

"It is impermissible, however, simply to engage in a hindsight reconstruction of the claimed invention using the Applicant's structure as a template and selecting elements from the references to fill the gaps". *In re Gorman*, 933 F. 2d 982, 987, 18 USPQ 2d 1885 (Fed. Cir. 1991).

B. Grouping of the claims

For the first ground of rejection contested by appellant in this appeal, claims 15-16, 18 may be treated as one group, and independent claim 15 may be taken as the representative for the issue on appeal. For the second ground of rejection contested by appellant in this appeal, claims 15, 17 & 19 may be treated as one group to stand or fall together, and independent claim 15 may be taken as the representative for the issue on appeal. For the third ground of rejection contested by appellant in this appeal, claims 15 and 20, and claim 15 may be taken as the representative for issue on appeal.

C.

Claims 15-16 and 18 were improperly rejected under 35 U.S.C. 102(e) as being anticipated by Ono et al. (2002/0107129, Ono hereinafter).

1. The rejection

In the Office Action mailed on 10/13/2005, claims 15-16 and 18 were rejected under 35 U.S.C. 102(e) as being anticipated by Ono et al. (2003/0107129, Ono hereinafter). In making the rejection, the Examiner contends that Ono discloses providing a chip 15 with an active surface (top surface) having plurality of bonding pads 16 thereon and a backside (bottom side). The Examiner also asserts that Ono teaches forming at least a bump pad 14 on the backside of the chip and forming a bump 19 to the bump pad. The Examiner further argues on pg. 5 of Office Action that Ono teaches in Figure 2 that "the bump pad 14 is formed on the backside of the chip and the bump 19 is electrically formed on the pad".

2. The prior art

The prior art reference Ono relates to a method for fabricating a resin-encapsulated semiconductor device. The method of Ono includes forming a first interconnect pattern 11 and a first dielectric layer 12 covering the top and side surfaces of the first interconnect pattern 11 as shown in Figure 2. A second interconnect pattern 14 is then formed on the first dielectric layer 12 and is connected to the first interconnect patter 11 via through holes 13 in the first dielectric layer 12. Ono '129 also teaches that a semiconductor chip 15 is mounted on the first dielectric layer 12 [0028] and bonding wires 17 connect the chip electrodes 15 on the semiconductor chip 11 with the second interconnect pattern 14. Ono '129 specifically clarifies in [0029] that the second interconnect pattern 14 located above the through holes 13 is formed on an area other than the area where the semiconductor chip 15 is mounted. Further, the bumps 19 of Ono are formed on the bottom surface of the first interconnect pattern 11 [0028].

In brief, Ono teaches **mounting the semiconductor chip 15 on the first dielectric layer 12**, and the **second interconnect pattern 14 is also formed on the first dielectric layer 12.** Moreover, **the second interconnect pattern is formed on an area other than the area where the semiconductor chip 15 is mounted**.

3. The prior art differentiated

What significantly distinguishes the structure of this invention from the prior art references is that the present invention teaches providing a chip with a backside with at least a bump pad being formed on the backside of the chip and forming a bump on the bump pad on the backside of the chip. As clearly demonstrated in Ono, at least the above claimed features were not taught or suggested.

Contrary to the Office's assertions, Ono does not teach forming a bump pad on the backside of the chip. In fact, Ono teaches that both the semiconductor chip 15 and the second interconnect pattern 14 (alleged as comparable to the chip and bump pad of the instant case), are both formed on the first dielectric layer 12. Further, Ono emphasizes that the second interconnect pattern 14 is located on an area other than the area where the semiconductor chip 15 is mounted. Accordingly, the second interconnect pattern 14 of Ono '129 can not be formed on the semiconductor chip 14. In fact, the second interconnect pattern 14 and the semiconductor chip 15 of Ono '129 are not even physically connected to each other or disposed above one another, but are merely eclectically connected to each other through bonding wires 17. In other words, Ono '129 fails to teach forming a bump pad on the backside of the chip.

Further, Ono '129 is completely silent about forming a bump on the bump pad. Ono '129 specifically teaches in [0028] that the metallic bumps 19 are formed on the bottom surface of the first interconnect pattern 11. The Examiner, however, argued in the Paper dated October 13, 2005 that the bump 19 of Ono is "electrically formed on" the pad (the second interconnect pattern 14). Appellant is puzzled about the Examiner's implication of "electrically formed on". Although the first interconnect pattern 11 of Ono '129 is electrically connected to the second interconnect pattern 14 through the through-holes 13, the bumps 19 are still not formed on the second interconnect pattern 14 (the alleged bump pad) and are only electrically connected to the second interconnect pattern 14 through both the first interconnect pattern 11 and the through-holes 13. In brief, the bumps 19 are formed on the first interconnect pattern 11 and not on the second interconnect pattern 14.

Accordingly, Appellant respectfully asserts that the prior art reference fails either expressly or inherently described each and every element of the claim in issue to render the claim in issue anticipated.

4. Examiner's Response to the above arguments

In the Examiner's Answer issued July 10, 2006, the Examiner again alleged that Ono's conductive pattern 14 is the same as the bump pad since it provides electrical connections between the bump 19 and the semiconductor chip 15 through the intermediate element 13. The Examiner further referred to Ono's Figures 2-3 and insisted that the chip must be formed on at least a portion of the pattern 14 on the backside and within the perimeter of the chip since element 13 is directly connected to the pattern 14 at one end as shown in Figure 2 of Ono '129. The Examiner was of opinions that Ono's teachings related to paragraph [0029] should be interpreted as "portion of the pattern 14 protrudes outside of the area where the chip is mounted" and "[t]he bottom of the chip is obviously not formed on this protruded portion of pattern 14".

In addition, the Examiner interpreted that the phrase "formed on" does not exclude anything in between. The Examiner admitted that bump 19 of Ono '129 is not directly formed on the element 14, but stated that the claim of this application does not explicitly require the bump to be formed directly on the pad.

5. Appellant's reply and arguments to the Examiner's Response

As taught clearly by the relied reference Ono '129, "A second interconnect pattern 14 is formed on the first dielectric layer 12 ..... A semiconductor chip 15 is mounted on the first dielectric layer 12, ..." (paragraph [0028]).

Although the Examiner insisted relying on Figure 2 of Ono '129 for supporting the formation of the pattern 14 on the backside of the chip 15, the teachings of Ono are in fact contradict to its own Figure 2. Especially, according to Figure 3 (the top plan view of the first interconnect pattern 11 of Figure 2), the bumps 19 are located on the outer portions of the pads 31 and, contrarily, the through-holes 13 are connected to the inner portions of the pads 13. Clearly, the locations of the through-holes 13 and the bumps 19 are not overlapped at all, and **none of the through-holes 13 are aligned with or located right above the bumps 19, *which says the opposite to the images of Figure 2***. Further referring to Ono's Figure 4B (top plan view of the second interconnect pattern 14 of Figure 2), the through-holes 13 are connected to the inner portions of the inner pads 32 of the second interconnect

pattern 14. Also from Ono's contexts (paragraph [0030]), "Each pad 32 has an inner portion located **in the vicinity** of the location where the semiconductor chip 15 is mounted ...". In conjunction with Ono's teachings in paragraph [0029], "[s]ince the second interconnect pattern 14 located above the through-holes 13 is formed on an area **other than** the area where the semiconductor chip 15 is mounted, the through-holes 13 are also formed on an area other than the area where the semiconductor chip 15 is mounted.", it is clear that the second interconnect pattern 14 is disposed on the first dielectric layer 12 and on an area other than where the semiconductor chip 15 is mounted.

The Examiner's arguments are unsubstantiated by simply relying on the dubious Figure 2 of Ono '129 but ignoring the other related top view figures (Figures 3-4B) and their related descriptions stated by Ono '129.

In response to the lines 4-6 of the first paragraph in page 7 of the Examiner's Answer, Appellant respectfully points out that "the bumps 19 are in an array on almost the whole area of the bottom surface of the semiconductor device" as taught by Ono '129 (paragraph [0029]), rather than the bottom surface of the semiconductor chip 15 as asserted by the Examiner.

In brief, as the relative positions depicted by Ono's Figure 2 are inconsistent with the top view figures (especially Figure 3) and contradict to the related descriptions in the contexts of Ono '129, it is reasonable to doubt the credibility of Ono's Figure 2. In fact, if considering the teachings of Ono '129 as a whole and in reference to Ono's other figures (Figures 3-4B), it is concluded that Ono's second interconnect pattern 14 is not formed on the backside of the chip 15. Therefore, Ono '129 fails to teach forming a bump pad on the backside of the chip.

In addition, even though the Examiner admitted that bump 19 of Ono '129 is not directly formed on the pattern 14, the Examiner still alleged that Ono's pattern 14 provides electrical connections to the bumps 19 and can be characterized as a bump pad (the first paragraph in page 6 of the Examiner's Answer). However, to any one of ordinary skills in the art, since the pattern 14 and the bumps 19 are not even physically connected, the pattern 14 would not be considered as bump pads but merely one of the interconnect layers.

Accordingly, Appellant respectfully asserts that the prior art reference Ono '129 fails either expressly or inherently described each and every element of the claim in issue to render the claim in issue anticipated.

D. *Claims 17 and 19 were improperly rejected under 35 U.S.C. 103(a) as being unpatentable over Ono as applied to claims 15-16 above, and further in view of Akram (US 6,861,763)?*

1. The rejection

Claims 17 and 19 have been rejected under 35 USC §103(a) as being unpatentable over Ono as applied to claims 15-16 above, and further in view of Akram. In making the rejection in the Office Action dated October 13, 2005, the Examiner has concluded that Ono discloses all of the claimed invention, except the mask has at least an opening so that the backside of the chip is exposed. The Examiner then asserts that Akram discloses in Figure 6A an analogous package includes chip 12 pad 14, mask 30c wherein the mask layer or passivation layer has an opening so the chip is exposed and forming a metallic layer over the mask and the exposed portion of the chip, and the mask or passivation layer is further removed to form a solder ball therein.

2. The prior art

The prior art reference Arkam teaches forming an array of bond pads 14 at active surface 16 of each die 12 (col. 7, ln. 50-55, Figure 2), attaching conductive structures 18 such as conductive bumps or pillars to bonding pads as shown in Figure 3, and polymerizing a protective layer 30 in situ over active surface 16, including within interstitial spaces between adjacent bond pads 14 or conductive structures 18 as shown in Figure 6 and 6A and discussed in col. 8, ln. 25-31.

3. The prior art differentiated

Similar to Ono, Akram also fails to teach forming a bump pad on the backside of the chip and forming a bump on the bump pad. Instead, Akram specifically teaches forming the bump pads 14 and bumps 18 on the active side 16 of the chip.

Moreover, Arkam does not teach putting a mask on the backside of the chip exposing the backside of the chip, forming a metallic layer over the mask and the exposed backside of the chip and removing the mask so that the remaining metallic layer on the backside of the chip becomes the bump pad. Instead, Akram teaches forming the bump pad 14 first on the active surface, and forming the bumps 18 thereon. Only subsequent to the forming of the pads 14 and the bumps, the protective layer 30 is then polymerized on the active surface between the adjacent bond pads 14 or conductive structure 18.

4. Even if combined Ono and Akram

Since neither Ono nor Akram teaches or suggests at least forming at least a bump pad on the backside of the chip and forming a bump on the bump pad, Appellant respectfully submits that claim 15 defines over the prior art references for at least the reasons discussed above. If the independent claim 15 is allowable over the cited references, its independent claims 17 and 19 are allowable as a matter of law, because these dependent claims contain all features of their respective independent claim 15. Further, not only Akram fails to teach forming bump pad on the backside of the chip, Akram actually teaches the steps of forming the bump pad on the chip in the order reversed of those taught in claims 17 and 19. Therefore, even if Ono were combined with Akram, the combination still can not possibly render the method of fabricating bumps on a backside of a chip of the claimed invention obvious.

5. The Examiner's Response to the above arguments

In the Examiner's Answer issued July 10, 2006, it again alleged that Akram teaches the mask layer 30C on the backside of the chip or die 12 as a protection layer, thus comparable to the mask layer of this invention.

6. Appellant's reply and arguments to the Examiner's Response

According to Akram's Figures 6-6A, the pads 14 and the bumps 18 are mounted on the active surface 16 of the die 12. Moreover, as stated by Akram, "[a] layer 30 of protective material having a planar upper surface 32 is formed on active surface 16 of die 12 including

between conductive structures 18 interstitial spaces 22." (Col. 7, lines 18-20) and "[t]he photopolymer material of first layer 30A adheres to active surface 16 of die 12. The process is repeated, forming additional layers 30B, 30C, 30D, 30E, 30F and 30G to sequentially build layer 30 covering active surface 16 ..." (Col. 8, lines 37-41), either layer 30 or layer 30A is formed on the active surface 16 of die 12, instead of the backside of the chip. Clearly, it is unlikely to consider layer 30 or 30C of Akram being comparable or equivalent to the mask disposed on the backside of the chip as recited in claim 17 of this invention.

E. *Claim 20 was improperly rejected under 35 U.S.C. 103(a) as being unpatentable over Ono as applied to claims 15-16 above, and further in view of Koh (US 2004/0135266)?*

1. The rejection

Claim 20 has been rejected under 35 USC §103(a) as being unpatentable over Ono as applied to claims 15-16 above, and further in view of Koh. In making the rejection in the Office Action dated October 13, 2005, the Examiner has contended that Ono discloses all of the claimed invention, except for using a wire-boding machine in the process of making the electrical connection elements.

2. The prior art

The prior art reference Koh basically teaches a substrate of non-electrically conducting material for mounting a semiconductor chip.

3. The prior art differentiated

Similar to Ono, Koh also fails to teach or suggest forming at least a bump pad on the backside of the chip and forming a bump on the bump pad.

4. Even if combining Ono and Koh

Since neither Ono nor Koh teaches or suggests at least forming at least a bump pad on the backside of the chip and forming a bump on the bump pad, Appellants respectfully submit that claim 15 defines over the prior art references for at least the reasons discussed above. If the independent claim 15 is allowable over the cited references, its dependent claim

20 is allowable as a matter of law, because the dependent claim contains all features of their respective independent claim 15. Accordingly, Ono and Koh, neither alone nor in combination can possibly render the method of fabricating bumps on a backside of a chip of the claimed invention obvious.

F. Conclusion

As noted, the Examiner has not properly applied 35 U.S.C. § 102 and U.S.C. § 103 in his rejections of the claims at issue. Accordingly, Appellants believe that the rejections under 35 U.S.C. § 102 and U.S.C. § 103 to be in error, and respectfully request the Board of Appeals and interferences to reverse the Examiner's rejections of the claims on appeal.

Date : Sept. 8, 2006

Respectfully Submitted,

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VIII. Claims appendix

CLAIMS ON APPEAL:

Claims 1-14. **Cancelled.**

Claim 15. (previously presented) A method of fabricating bumps on a backside of a chip, comprising the steps of:

providing the chip with an active surface having at least a bonding pad thereon and the backside;

forming at least a bump pad on the backside of the chip; and

forming a bump on the bump pad.

Claim 16. (original) The method of claim 15, wherein the step of forming the bump pad on the backside of the chip further comprises:

forming a metallic layer on the backside of the chip; and

patterning the metallic layer to form the bump pad.

Claim 17. (original) The method of claim 15, wherein the step of forming the bump pad on the backside of the chip further comprises:

putting a mask on the backside of the chip, wherein the mask has at least an opening so that the backside of the chip is exposed;

forming a metallic layer over the mask and the exposed backside of the chip; and

removing the mask so that the remaining metallic layer on the backside of the chip becomes the bump pad.

Claim 18. (original) The method of claim 15, wherein before forming the bump pad on the backside of the chip, the method further comprises forming a protective film on the active surface of the chip.

Claim 19. (original) The method of claim 15, wherein the chip further comprises a passivation layer coated on the backside of the chip so that the passivation layer is removed before forming the bump pad on the backside of the chip.

Claim 20. (previously presented) The method of claim 15, wherein the step of forming the bump on the bump pad comprises performing one process selected from the group consisting of a patterning and electroplating process, a printing process, a bump-bonding process by a wire-bonding machine and a ball-implanting process.

IX. Evidence appendix

There is no evidence submitted pursuant to §§ 1.130, 1.131, or 1.132 of this title or of any other evidence entered by the examiner and relied upon by appellant in the appeal, along with a statement setting forth where in the record that evidence was entered in the record by the examiner.

V. Related proceedings appendix

There are no decisions rendered by a court or the Board in the proceeding identified in the Related Appeals and Interferences section of the brief.